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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,800	08/24/2001	Paul Jeffrey Garnett	5681-03000	2174

7590 01/05/2005

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EXAMINER	
DUNCAN, MARC M	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,800	GARNETT ET AL.	
	Examiner	Art Unit	
	Marc M Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30-35* is/are allowed.

6)☒ Claim(s) *1,2,6-21 and 25-29* is/are rejected.

7)☒ Claim(s) *3-5 and 22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

NADEEM IQBAL
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

Status of the Claims

Claims 1, 2, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20, 21, 26, 27, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of IEEE – "parity check."

Claims 6, 13 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams and IEEE – "parity check" as applied to claims 1, 10 and 20 above, and further in view of IEEE – "word (6)."

Claims 3, 4, 5, 22, 23 and 24 are objected to.

Claims 30-35 are allowed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20, 21, 26, 27, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of IEEE – "parity check."

Regarding claims 1 and 7:

Williams teaches a dirty memory being operable to store dirty indicators in col. 5 line 66-col. 6 line 3.

Williams teaches each dirty indicator being settable to a given value indicative that a block of memory associated therewith has been dirtied in col. 5 line 66-col. 6 line 3.

Williams teaches said dirty indicators being stored in groups in col. 2 lines 60-62. The dirty indicator bits are necessarily stored in the dirty RAM in at least one group.

Williams does not explicitly teach each group having associated therewith a validity indicator computed from the dirty indicator values of the group, the control logic being operable on reading a said group to compute a validity indicator value based on the dirty indicator values for the group to determine the integrity of the group. Williams does, however, teach a dirty memory that stores information on dirtied memory pages in order to re-sync lockstep processors.

IEEE – "parity check" explicitly teaches the use of a parity check for a group of bits in order to determine the integrity of the bits on page 794 "parity check."

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the parity check of IEEE – "parity check" with the dirty memory of Williams.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Williams teaches that the dirty ram is necessary for a fault tolerant computing system. Williams expresses a need for the dirty ram to have a high level of reliability and integrity in col. 7 lines 50-53. This need is met by a parity check, as defined by IEEE – "parity check". The parity check computes an indicator value when a group of bits is read and compares the value against a previously computer parity value, thereby determining the integrity of the information read.

Regarding claims 2 and 12:

IEEE – "parity check" teaches wherein the validity indicator is a parity indicator on page 794 "parity check."

Regarding claims 7 and 14:

Williams teaches wherein each dirty indicator comprises a single bit in col. 6 lines 8-10.

Regarding claims 8 and 15:

IEEE – "parity check" teaches wherein a validity indicator comprises a single bit on page 794 "parity check."

Regarding claims 9 and 16:

Williams teaches wherein a block of memory is a page of main memory in col. 6 lines 8-10.

Regarding claim 11:

IEEE – "parity check" teaches the dirty memory of claim 10 configured to re-compute the validity indicator for a group each time a dirty indicator in the group is

changed on page 794 "parity check." This function is inherent in a parity bit. In order to be accurate and to allow for error recovery, the parity must necessarily be recomputed each time a member of the parity group is changed.

Regarding claim 17:

See the above citations for claims 1 and 10.

Williams also teaches at least one processing set that includes main memory in col. 1 lines 16-22.

Regarding claim 18:

Williams teaches a plurality of processing sets that each includes main memory in col. 1 lines 16-22.

Regarding claim 19:

Williams teaches wherein the processing sets are operable in lockstep, the computer system comprising logic operable to attempt to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error in col. 2 line 63-col. 3 line 10.

Regarding claim 20:

See the above rejections of claims 1 and 10.

Williams also teaches a plurality of processing sets of a fault tolerant computer system in col. 1 lines 16-22 and the Title.

Williams further teaches the performance of at least one cycle of copying any block of memory that has been dirtied from a first processing set to each other processing set in col. 6 line 66-col. 7 line 11.

Regarding claim 21:

IEEE – "parity check" teaches wherein the validity indicator is a parity indicator on page 794 "parity check."

Regarding claim 26:

Williams teaches wherein each dirty indicator comprises a single bit in col. 6 lines 8-10.

Regarding claim 27:

IEEE – "parity check" teaches wherein a validity indicator comprises a single bit on page 794 "parity check."

Regarding claim 28:

Williams teaches wherein a block of memory is a page of main memory in col. 6 lines 8-10.

Regarding claim 29:

IEEE – "parity check" teaches the dirty memory of claim 10 configured to re-compute the validity indicator for a group each time a dirty indicator in the group is changed on page 794 "parity check." This function is inherent in a parity bit. In order to be accurate and to allow for error recovery, the parity must necessarily be recomputed each time a member of the parity group is changed.

Claims 6, 13 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams and IEEE – "parity check" as applied to claims 1, 10 and 20 above, and further in view of IEEE – "word (6)."

Regarding claims 6, 13 and 25:

See the teachings of Williams and IEEE – "parity check" above.

Williams and IEEE – "parity check" do not explicitly teach wherein a group of dirty indicators plus the validity indicator occupy one memory word. Williams and IEEE – "parity check" do, however, teach the use of parity with blocks.

IEEE – "word (6)" explicitly teaches wherein a group of dirty indicators plus the validity indicator occupy one memory word on page 1283 "word (6)."

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the word teaching of IEEE – "word (6)" with the parity block teaching of Williams and IEEE – "parity check."

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because a word is simply defined as a sequence of bits or characters that is stored, addressed, transmitted and operated on as a unit within a given computer. It would be therefore be obvious for a parity bit and the group of bits with which the parity bit is associated to be a word because they are a sequence of bits that is operated on as a unit.

Response to Arguments

Applicant's arguments filed 10/18/2004 have been fully considered but they are not persuasive.

In response to applicant's arguments that the references, either alone or in combination, fail to teach that the dirty indicators are stored in groups, the examiner respectfully disagrees.

Williams teaches a dirty memory that stores dirty bits that represent pages of memory. These bits are necessarily organized in one or more groups, the word group being defined in Webster's Collegiate Dictionary as "an assemblage of objects regarded as a unit." Further, the used of a parity check in combination with the dirty memory inherently includes a teaching of bits stored in groups. One of ordinary skill in the art at the time of invention understood that the use of a parity check necessarily requires the bits on which the parity check is being performed to be organized in groups. Without the dirty indicators being organized in groups a parity check would have been impossible.

In response to applicant's arguments that the references, either alone in combination, fail to teach that the control logic computes a validity indicator value on reading a group to determine the integrity of the group, the examiner respectfully disagrees.

It is inherent to the function of a parity check to recomputed parity upon reading a group. The only way for parity to function is to compute the parity of the group and compare it to the stored parity indicator in order to determine if a bit has changed.

In response to applicant's arguments that there is no suggestion that a parity check could or should be applied in the field of dirty memory, the examiner respectfully disagreed.

As stated above, Williams expresses an explicit desire for the dirty RAM to have a high level of reliability and integrity. The parity check, as taught by IEEE, meets that

explicit desire by providing a system to ensure the reliability and integrity of groups of bits, which is what the dirty RAM of Williams stores.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-T and TH-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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